Thermal Analysis of a 3D Die-Stacked High-Performance Microprocessor

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ABSTRACT

3-dimensional integrated circuit (3D IC) technology places circuit blocks in the vertical dimension in addition to the conventional horizontal plane. Compared to conventional planar ICs, 3D ICs have shorter latencies as well as lower power consumption, due to shorter wires. The benefits of 3D ICs increase as we stack more die, due to successive reductions in wire lengths. However, as we stack more die, the power density increases due to increasing proximity of active (heat generating) devices, thus causing the temperatures to increase. Also, the topmost die on the 3D stack are located further from the heat sink and experience a longer heat dissipation path. Prior research has already identified thermal management as a critical issue in 3D technology. In this paper, we evaluate the thermal impact of building high-performance microprocessors in 3D. We estimate the temperatures of a planar IC based on the Alpha 21364 processor as well as 2-die and 4-die 3D implementations of the same. We show that, compared to the planar IC, the 2-die implementation and 4-die implementation increase the maximum temperature by 17 Kelvin and 33 Kelvin, respectively.

Categories and Subject Descriptors

B.7 [**Integrated Circuits**]: Advanced technologies

General Terms

Reliability, Experimentation

Keywords

Thermals, 3D Technology, Power density

1. INTRODUCTION

3D integrated circuit (3D IC) technology greatly reduces wire lengths [1] thus providing faster on-chip communication. 3D IC technology places planar circuit blocks in the vertical dimension and connects the blocks with a high-density and low-latency interface. Two functional blocks connected by a global wire in a planar IC can instead be stacked to drastically reduce the wire lengths. Wire-dominated functional blocks such as caches and register files can be stacked on top of themselves to reduce intra-block wiring [2, 3, 4]. Reducing the amount of wire can also have a significant impact on power consumption [5]. 3D technology provides the dual benefits of reduced latency and reduced power dissipation. Current high-performance processors are increasingly being constrained by the wire RC delays [6] and power dissipation [7], thus making 3D integration technology an appropriate new technology for building processors. Processor companies are actively researching the 3D technology [8, 9, 10, 11]. Academic research effort has focused on the circuit implementation, process technology, physical design and automated design tools [12, 13, 14, 15, 16, 2, 17].

The benefits of 3D ICs increase as we stack more die, due to successive reductions in wire lengths. However, as we stack more die, the power density increases due to vertical stacking of the active devices and reduced die footprint, thus causing the on-chip temperatures to increase. Also, the topmost die on the 3D stack are located further from the heat sink and experience a longer heat dissipation path in the vertical direction to the heat sink. Increased power density has made thermal management to be identified as a critical issue in 3D technology [18]. In this paper, we analyze the thermal impact of 3D IC technology on high-performance microprocessors by estimating the temperatures of a planar IC based on the Alpha 21364 processor as well as 2-die and 4-die 3D IC implementations of the same.

The rest of the paper is organized as follows. Section 2 provides a short background on 3D integration technology. Section 3 describes our high-performance processor model in planar and 3D technologies. Section 4 describes our experimental methodology. Section 5 presents our results and analysis. Section 6 discusses the related work. Section 7 summarizes our conclusions.

2. 3D INTEGRATION TECHNOLOGY

There are different types of 3D integration technologies based on the styles of fabrication. A majority of the 3D technologies fall under one of the two categories, namely die-bonding and Multi-layer Buried Structures (MLBS) [3]. The die-bonding 3D technology processes the circuits using conventional 2D fabrication processes and uses metal vias

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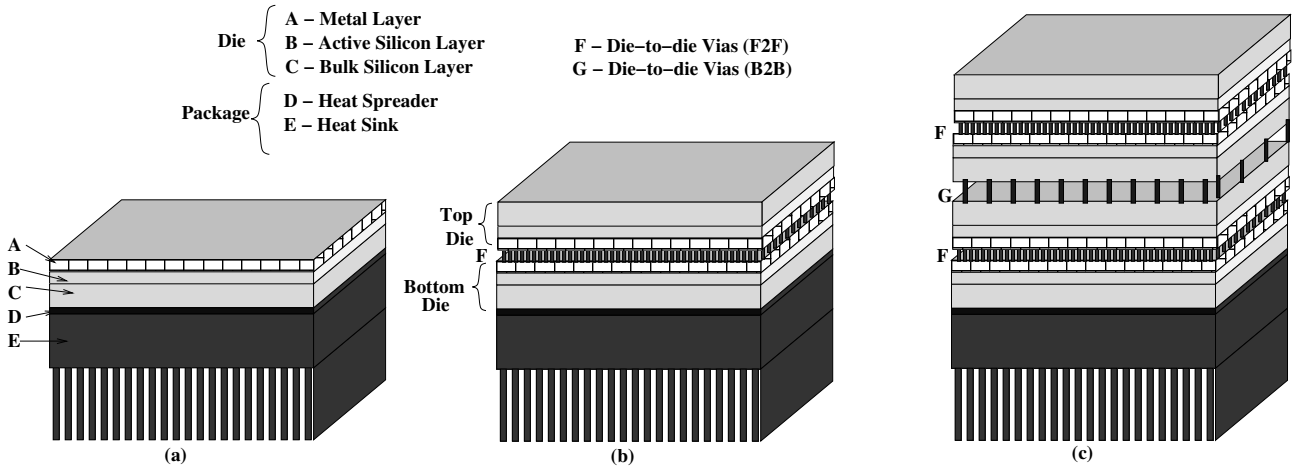

Figure 1: (a) A planar IC (b) A 3D IC with 2-die (c) A 3D IC with 4-die

to bond the planar die vertically [19, 20]. In this paper, we model a die-bonding 3D integration technology that vertically stacks planar die and bonds them at the interface through metal stubs (die-to-die vias). Figure 1(a) shows a conventional planar IC modeled as five layers: metal layers (A), active silicon (B), bulk silicon (C), heat spreader (D) and heat sink (E). The heat spreader is attached to the bulk silicon with a thermal interface material [21]. Figure 1(b) shows a 2-die 3D IC built with two planar die stacked with their metal layers face-to-face (F2F). There can be three different stacking topologies for interfacing multiple planar die namely, face-to-face (F2F), face-to-back (F2B) and back-to-back (B2B). The different topologies have different quality and pitch of the die-to-die (D2D) vias at the interfaces and thus influence the benefits obtained from building a 3D IC. Current 3D technology supports $\sim 2\mu$m F2F vias and $\sim 4\mu$m B2B vias [22]. For the 2-die 3D IC with the F2F topology shown in Figure 1(b), D2D vias are etched and deposited on top of the metal layer of each of the planar die using conventional metal etching technology. Therefore, the via pitch can be as dense as regular on-die interconnects, and the realizable pitch is only limited by the accuracy of aligning the two die. The two die are aligned so that the vias line up vertically and bonded using thermocompression to fuse the vias on the two die [23]. The die-to-die via interface is densely populated since the vias are required as the physical bonding mechanism independent of whether they actually carry a signal. The bulk silicon layer of the top die is thinned down with chemical-mechanical polishing down to only $\sim 10\mu$m allowing low impedance backside vias to be etched through, which provide I/O and power/ground connections.

Figure 1(c) shows a 4-die 3D IC that combines two F2F 2-die stacks with a B2B interface between the pairs of die. Vias are etched through the thinned backside silicon of the intermediate die to provide connectivity from one pair to the other. In the rest of the paper, we model the 2-die and 4-die 3D ICs as shown in Figure 1(b) and Figure 1(c), respectively.

3. PROCESSOR MODEL

In this section, we describe our models for the planar and 3D IC implementations of a high-performance processor. Figure 2 shows our baseline model based on the Alpha

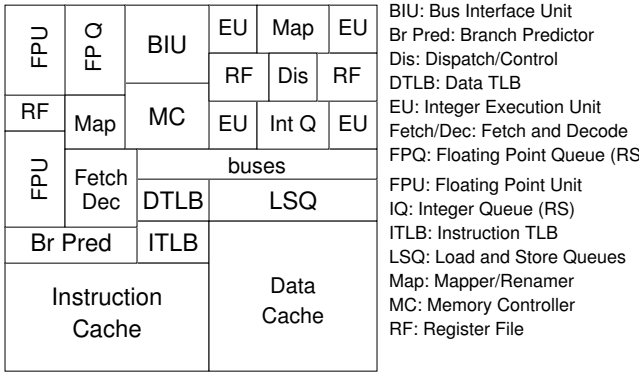

Figure 2: Baseline processor based on the Alpha 21364 (L2 cache not shown)

21364. We assume a 70 nm technology [24] with a supply voltage of 0.9 volts and copper metallization with eight metal layers.

We model the 3D implementations of our baseline processor by either partitioning and stacking the planar functional blocks such that a part of each functional block resides on each stacked die or by stacking the whole units on one of the die depending on benefits and feasibility.

For the 2-die stacked 3D IC implementation, we partition and stack the SRAM-based blocks such as caches and register files such that half the entries are on each of the die [2, 3]. 3D self-stacking of functional blocks with half the entries on each of the die, halves the wires running across the entries and thus reduces the latency and power consumption of those blocks. Similarly, we stack the CAM-based blocks such as instruction schedulers with half the entries on each die. CAM-based structures include a broadcast mechanism that has a high amount of wire complexity. With 3D stacking, the wire complexity greatly reduces and lowers both the latency and power consumption. Combinational logic blocks such as arithmetic and logical units are split such that either half the operands are processed on each of the die or whole units are placed on one of the stacked die depending on benefits and feasibility. Note that the 3D partitioning

Material	Specific heat capacity (SHC) $J/m^3/K$	Thermal resistivity (TR) $(W/m/K)^{-1}$
Cu	3.49E+6	2.53E-3
Si	1.75E+6	0.01
SiO_2	1.79E+6	1.69
Air	1.51	40

Table 1: Material properties

of logic-intensive structures such as adders may not in itself provide significant latency and power benefits. But the partitioning of arithmetic units might in turn significantly reduce the wire-intensive bypass network that is needed to communicate the results generated by the arithmetic units among themselves. For the 4-die 3D IC implementation, we similarly partition each microarchitectural block into four subblocks to be placed on each of the four stacked die. With such partitioning, the 2-die (4-die) stacked 3D IC will have approximately half (quarter) the footprint as the planar IC.

4. EXPERIMENTAL METHODOLOGY

We use a thermal simulation tool called HotSpot 3.0 from the University of Virginia [25] for thermal simulations. HotSpot can model multiple layers of silicon and metal required to model a 3D IC. HotSpot takes power consumption data and layer parameters as inputs and generates the steady state temperatures for various functional blocks. Using HotSpot, we simulate each die as three layers: bulk silicon, active silicon, and the metal layer. We compute an average specific heat capacity (SHC) and thermal resistivity (TR) of the metal layer taking into account the proportion of the metal and inter-layer dielectric on each of the layers. We obtained the material properties, listed in Table 1 from the CRC handbook [26]. For the interface between adjacent die, we compute an average SHC and an average TR based on the fraction of the interface that is occupied by copper versus air. We model the D2D via width to be half of the via pitch, which results in a 25% copper occupancy (75% air) at the die-to-die interface. We use a phase change metallic alloy [21] for the thermal interface material (TIM) between the bulk silicon layer of the last die and the heat spreader. We use HotSpot's default heat spreader and heat sink models.

We have developed Spice circuit models of the 3D circuits and use it to generate the power consumption data for the 3D processor thermal simulations. We partition the planar functional blocks as explained in Section 3 to create the 3D ICs. Note that the 3D ICs have a smaller, denser footprint than the planar IC depending on the number of stacked die. We utilize the latency saving of 3D ICs to proportionally increase their clock frequency which in turn increases the power consumption.

We generated the power numbers for each functional block in a 70 nm [24] technology by scaling the power data provided by HotSpot for the planar configuration. We modified the configuration parameters and the layer parameters to represent our 3D ICs. We ran the simulations twice to collect the steady-state temperatures of the functional blocks. For the first simulation, we set the initial temperature to be 350 K. HotSpot takes the power trace data, the configuration parameters and the layer parameters and generates the steady state temperatures for various functional blocks. Then, we used those steady state temperatures as initial

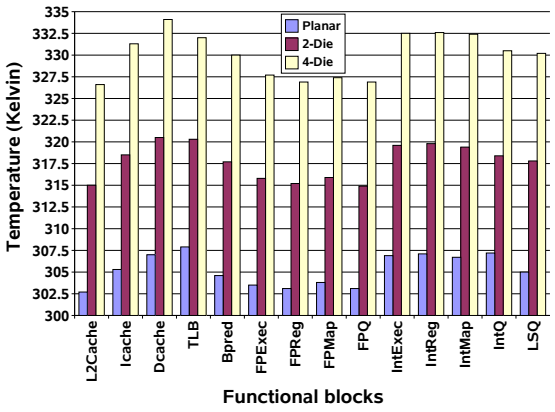

Figure 3: Temperatures of functional blocks on planar and 3D ICs

temperatures and regenerated the steady state temperature data. We present our results using this methodology in Section 5.

5. RESULTS

In this section, we present our thermal analysis of planar and 3D implementations of the high-performance processor. We begin by presenting the effect of power density on the 3D ICs.

5.1 Power Density Modeling

Based on our Spice circuit simulations of the 3D circuits, we assign the total power of the functional blocks to the 2-die and 4-die 3D ICs. Based on the self-stacking approach as explained in Section 3, we assume that the total power consumption of each of the functional blocks on the 3D IC is uniformly distributed among the corresponding stacked partitions of the block. As an example of our approach, if an arithmetic adder consumes a power of 300 milliwatts on the planar IC and our Spice circuit simulation of a 2-die stacked 3D adder shows a power reduction of 5% over the planar adder, we assign the power consumption of the 2-die 3D adder to be 285 milliwatts which translates to a power consumption of 142.5 milliwatts on each of the two stacked die. Note that our power calculation takes into account both the reduction due to reduced wire RC and the increase due to increased operating frequency. We similarly assign the power consumption of other functional blocks on each of the die. Note that this is a conservative assumption in terms of power density since it is possible to self-stack some circuit blocks such that only one of the stacked partitions is active at any given time. For example, consider a planar cache that has 256 lines. The 2-die 3D implementation stacks 128 lines on each die. The address decoding logic of the 3D cache selects only one of the two die based on the input address. Thus, the address decoding logic generates activity and power dissipation on only one of the die, thus cutting the overall switching power roughly in half. This power reduction might offset the halving of the 3D footprint and cause the 3D power density to be roughly the same as that of the planar processor. Also, if different functional blocks are vertically stacked, they may not both be actively dissipating power simultaneously. For example, if

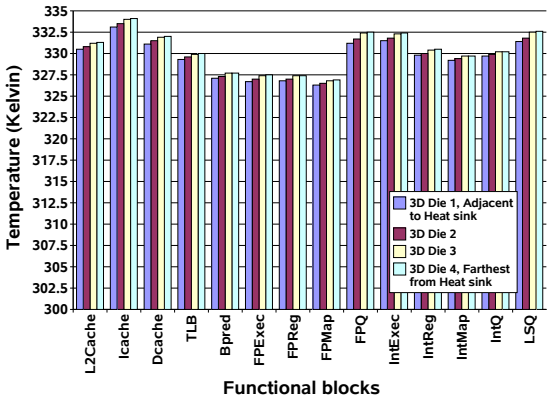

Figure 4: Temperatures on each of the four die on a 4-die stacked 3D IC

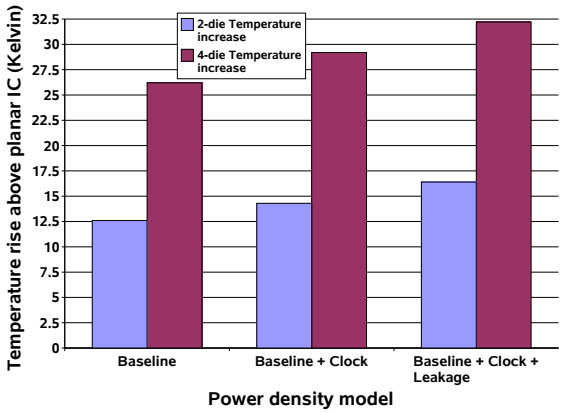

Figure 5: Maximum Temperature Increase with Clock and Leakage Power Modeling

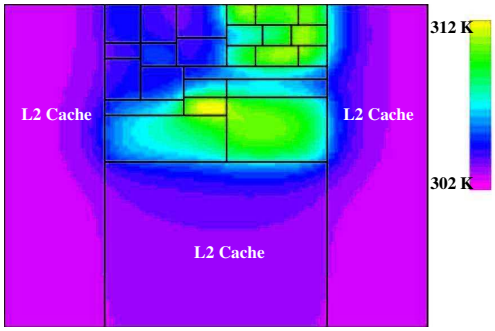

Figure 6: Thermal Profile of the Planar Processor

an integer adder is stacked on an integer multiplier, only one of them might be active based on the application requirements. Thus, distributing the power of each of the 3D circuit blocks uniformly among the stacked die is a conservative power density model.

Figure 3 shows the die temperatues of planar and 3D ICs based on our thermal analysis. From Figure 3, the maximum temperature on the planar IC is 307.9 K. The corresponding maximum temperatures on the 2-die and 4-die 3D implementations are 320.5 K (12.6 K increase over the planar IC) and 334.1 K (26.2 K increase over the planar IC), respectively. Note that the rough doubling of the power density experienced by the 3D ICs has lead to only a moderate increase (12.6 K and 26.2 K for 2-die and 4-die ICs, respectively) in the maximum on-chip temperatures. The maximum temperatures from our experiments is in contrast to the data published by prior research where the 2-die 3D ICs are reported to increase the on-chip temperatures by as much as 50 K [27, 28]. The large difference in the reported temperatures can be explained by the fact that we include modeling of vias, that serve as efficient heat dissipation paths and also that our model is built using the current advancements such as copper metallization and efficient packaging materials [21].

5.2 Temperatures on stacked die

We compare the temperatures on the individual die of the 4-die 3D IC. Figure 4 shows the temperatures of the functional blocks on each of the four die on the 4-die 3D IC. From Figure 4, we see that, for each functional block, the die that are further away from the heat sink have a slightly higher temperature than the die that are closer to the heat sink. But the overall difference in temperatures among the individual die themselves is not large suggesting that the die interfaces are efficient at handling inter-die thermals.

5.3 Modeling Clock Power and Leakage Power

We refine the power density model by adding clock power and leakage power estimates to our high-performance processor. The Alpha processor has been reported to have the clock power to be 34% of the system power [29]. Since our baseline processor is based on the Alpha processor core, we assign the clock power to be 34% of the system power and correspondingly increase the power consumption of each of the functional blocks in both the planar and the 3D ICs. We model the leakage power to be 15% of the system power in a 70 nm technology based on the leakage power data in [30]. Note that we do not model the dependence of leakage power on temperature.

Figure 5 plots the increase over the planar IC temperature for the 3D ICs after taking the system clock power and the leakage power into account. From Figure 5, the maximum temperatures on the 2-die and 4-die 3D implementations increase by 16.4 K and 32.2 K, respectively over the planar baseline. The increased temperatures on the 3D ICs may require more aggressive cooling mechanisms [31], thus increasing manufacturing costs.

5.4 Thermal Profiles

In this section, we report the thermal profiles on the planar and 3D ICs. The thermal profile of the planar IC in Figure 6 shows the execution unit, the instruction TLB and data cache to be the hotspots. The thermal profile of the 3D IC with 2-die and 4-die are shown in Figure 7 and Figure 8, respectively. Although the 2-die and 4-die ICs have a smaller footprint compared to the planar, the profile sizes have been scaled up for clarity purposes. Note that the 3D ICs have similar thermal profiles as the planar IC. Figure 7 and Figure 8 show that the temperatures of individual functional blocks have increased as compared to the corresponding planar blocks. The temperatures on the 3D ICs are higher than the temperatures on the planar IC due to three reasons. One, the 3D ICs have a higher power den-

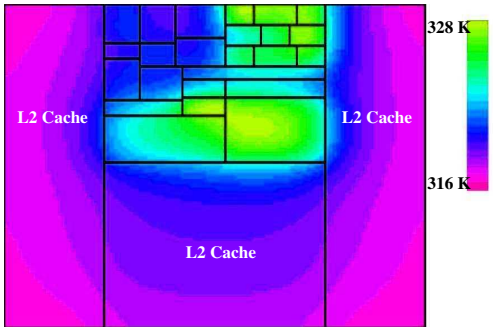

Figure 7: Thermal Profile of the 2-die 3D Processor

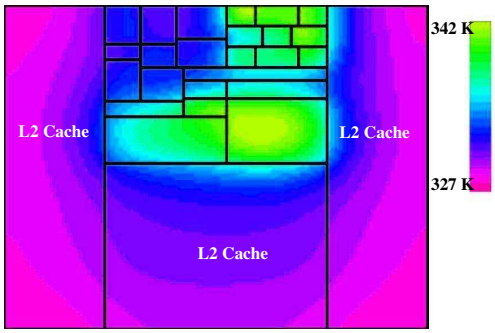

Figure 8: Thermal Profile of the 4-die 3D Processor

sity due to vertical stacking of the active devices. Two, the heat dissipation mechanism is less efficient in 3D ICs due to lower temperature gradients and longer heat dissipation paths to the heat sink. Three, the reduced die footprint of 3D ICs reduces the area of contact with the heat spreader and reduces the opportunity to convey the heat to the heat sink.

6. RELATED WORK

Thermal management is already a significant problem in current planar ICs and researchers are focusing efforts on building thermal-aware microarchitectures [32, 25]. There has been some recent work in the thermal analysis of 3D ICs [27, 28, 18]. Im et al. [28] derived analytical models for the thermal analysis of 3D ICs using data from the ITRS [33] and reported the temperature increase in 3D ICs to vary linearly with power density and as the square of the number of die. Our methodology uses Spice circuit simulations for latency and power estimates of circuit blocks and an existing thermal simulator for temperature estimates. Chiang et al. [27] considered heterogeneous 3D ICs and reported that the die temperatures on 3D ICs from thermal simulations are much lower if via effect is modeled, since vias serve as efficient heat dissipating paths. We model a homogeneous IC of a high-performance microprocessor with self-stacked circuit blocks. We factor the via effect as well as clock distribution power and leakage power in our thermal model. We use modern packaging solutions in our thermal model. Das et al. [18] analyzed the thermal behavior of two data-processing 3D circuits for FFT and DES and showed that the thermal performance of 3D ICs can be controlled by trading-off either energy or silicon area. In this paper, we analyze the thermal impact of the 3D technology on the design of high-performance microprocessors including SRAM-based and CAM-based circuit blocks as well as data-processing units.

7. CONCLUSIONS

3D integrated circuit (3D IC) technology greatly reduces wire latencies thus providing faster on-chip communication. The benefits of 3D ICs increase as we stack more die, due to successive reductions in wire delays. But increased power density and longer heat dissipation paths can cause the thermal behavior to worsen in 3D ICs. In this paper, we analyzed the thermal behavior of a high-performance microprocessor built with two die and four die in a 3D technology and showed that the temperature increases on the 3D implementations are much less than previously reported when we include modeling refinements such as via layers, copper metallization, and modern packaging materials. We demonstrated that the 3D implementations of our planar processor have similar thermal profiles as the planar IC.

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